In the Claims:

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) The method of claim [[1]] 13 wherein the ~~protruding 3D structure~~ bumps on said wafer comprise compliant elements.

4. (Currently Amended) The method of claim [[1]] 13 and further comprising:

removing the surface of the wafer with the bumps from the electrophoretic resist; and

patterning the electrophoretic resist after removing the ~~non-planar~~ surface of the wafer from the electrophoretic resist.

5. (Cancelled)

6. (Currently Amended) The method of claim [[5]] 14 wherein forming a plurality of conductors ~~second conductive layer~~ comprises:

forming a copper layer over portions of the seed layer not covered by the electrophoretic resist;

forming a nickel layer over the copper layer; and

forming a gold layer over the nickel layer.

7. (Currently Amended) The method of claim [[5]] 14 wherein the substrate comprises a semiconductor wafer and wherein forming a plurality of conductors ~~the second conductive layer~~ comprises a reroute layer electrically coupling a contact pad formed on the semiconductor wafer to a terminal on the ~~non-planar~~ surface of the wafer.

8. (Cancelled)

9. (Currently Amended) The method of claim [[1]] 13 and further comprising causing the ~~non-planar~~ wafer surface with the bumps to be moved relative to the electrophoretic resist while the ~~non-planar~~ wafer surface is ~~placed~~ in the electrophoretic resist.

10. (Currently Amended) The method of claim 9 wherein the ~~non-planar~~ wafer surface is rotated while the ~~non-planar~~ wafer surface is ~~placed~~ in the electrophoretic resist.

11. (Currently Amended) The method of claim 9 wherein the electrophoretic resist is stirred while the ~~non-planar~~ wafer surface is ~~placed~~ in the electrophoretic resist.

12. (Currently Amended) The method of claim [[1]] 4 and further comprising heating the substrate after removing the ~~non-planar~~ wafer surface from the electrophoretic resist.

13. (Original) A method for forming a plurality of three-dimensional structures on a substrate, the method comprising:

providing a wafer with bumps distributed on a surface of the wafer; and

forming a resist over the surface of the wafer including the bumps by coating the surface of the wafer with an electrophoretic resist by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic resist.

14. (Previously Presented) The method of claim 13 and further comprising:

patterning the resist to expose a seed layer over the surface of the wafer; and

forming a plurality of conductors over the exposed seed layer.

15. (Original) The method of claim 14 wherein the plurality of conductors electrically connect bonding pads on the wafer to terminals located on the bumps.

16. (Original) The method of claim 13 wherein the surface of the wafer is dipped into the electrophoretic resist in a horizontal arrangement of the wafer.

17. (Original) The method of claim 16 wherein a rear side of the wafer is protected from wetting during the process of dipping into the electrophoretic resist.

18. (Original) The method of claim 13 wherein the wafer is caused to rotate during the coating operation.

19. (Original) The method of claim 13 wherein a flow is produced at least below the wafer in the electrophoretic resist during the coating operation.

20. (Original) The method of claim 19 wherein the electrophoretic resist is caused to rotate in a region of the surface of the wafer.

21. (Original) The method of claim 20 wherein the rotation of the electrophoretic resist is produced by a stirrer.

22. (Original) The method of claim 13 wherein the wafer is removed in a horizontal position after the process of coating with the electrophoretic resist and the coating is baked thermally.